APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,372	01/16/2001	David F. Mchale	550-200	1910

23117	7590	06/01/2005

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EXAMINER
CHO, HONG SOL

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>21 January 2005</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-14 and 20* is/are allowed.

6)☒ Claim(s) *1-4,6-10 and 15-18* is/are rejected.

7)☒ Claim(s) *19,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
   application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   The following is a response to the amendments filed on 1/21/2005.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form

the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
> in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
> patent by another filed in the United States before the invention by the applicant for patent, except that an
> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
> subsection of an application filed in the United States only if the international application designated the United
> States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-4, 6-10 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by

Vadivelu (U.S 6629001).

        Re claims 1, 6, 15 and 18, Vadivelu discloses a controller controlling audio

channels by sending and receiving digital data streams at predefined time slots in a data

link (*a controller controlling interfacing to a data link, the data link enabling data to be

transferred in corresponding data slots,*) performing fixed rate of sampling (column 1,

lines 35-37). Vadivelu discloses a channel logic circuit with an input FIFO to buffer

input data (*each channel comprising a data buffer for storing data items,* column 4, lines

33-35). Vadivelu discloses a configuration register (*control register*) connected to the

buffer in the demultiplexer to store configuration data (*control data*) (*a control register

associated with the data buffer and arranged to store control data,* column 3, lines 48-

50). Vadivelu discloses a configuration register controlling the demultiplexer with buffers that will be enabled by configuration data such as the buffer enable signal (*the control data being settable to define for which data element or data elements are to be stored in that data buffer*, column 5, lines 35-39). Vadivelu discloses a controller controlling data transfer between audio channels and time slots by the control data (column 1, lines 35-38; column 5, lines 19-21). Vadivelu discloses the number of configuration registers and the channel logic circuits is less than the number of available audio channels (*the number of channels provided by the controller is less than the number of data elements whose data items are capable of being transferred by the data link*, column 3, lines 36-39).

Re claims 2, 3, 16, and 17, Vadivelu discloses steering the channel outputs from the channel logical circuits to any of the audio channels as selected by the corresponding select field in the configuration registers, storing data to the enabled input FIFO buffer (*data buffer of the channel is arranged to store data items relating to one or more data items as specified by the control data*, column 5, lines 26-36), and generating data to the data steering circuit (*transmitting data retrieved from the data buffer to the data slots of the data link*, column 6, lines 2-7).

Re claims 4 and 8, Vadivelu discloses a channel logic circuit with configuration registers (figure 2) and an input FIFO as a queue to buffer input data received from the audio channels (*to store data items to be transmitted on the data link*, column 4, lines 33-35) and an output FIFO as a queue to buffer output data to be sent to the audio channels (*to store data items received from the data link*, column 4, lines 26-28).

Re claim 7, Vadivelu discloses a controller connected to the codec via the data

link (column 3, lines 21-22).

Re claims 9 and 10, Vadivelu discloses a controller coupled to the system

memory with data (figure 1, element 130) via a processor (figure 1, element 105). It is

inherent that data will be transferred between the memory and the channel.

Allowable Subject Matter

4.   Claims, 19, 21 and 22 are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

5.   Claims 11-14 and 20 are allowable.

The following is an examiner's statement for reasons for allowance.

6.   Claim 11 and 19 are allowable over the prior art of record since the cited references taken

individually or in combination fail to particularly teach or fairly suggest <u>a method of</u>

<u>controlling interfacing to a data link, the data link enabling data items relating to a</u>

<u>number of data elements to be transferred in corresponding data slots of the data link, the</u>

<u>controller comprising: at least one channel, each channel comprising a data buffer for</u>

<u>storing data items, and a control register associated with the data buffer and arranged to</u>

<u>store control data, the control data settable to identify at least one data element whose</u>

<u>corresponding data items are to be stored in the data buffer; an interface mechanism for</u>

<u>controlling the transfer of data items between the at least one channel and the data slots of</u>

<u>the data link in dependence upon said control data; and a memory interface for coupling</u>

<u>the controller to a memory, to enable data items to be transferred between the memory</u>

and the at least one channel, wherein each control register has a first field settable to
indicate a compact mode in which data words passed between the associated data buffer
and the memory comprise a plurality of said data items.

Claims 13 and 21 are allowable over the prior art of record since the cited references
taken individually or in combination fail to particularly teach or fairly suggest a method
of controlling interfacing to a data link, the data link enabling data items relating to a
number of data elements to be transferred in corresponding data slots of the data link, the
controller comprising: at least one channel, each channel comprising a data buffer for
storing data items, and a control register associated with the data buffer and arranged to
store control data, the control data settable to identify at least one data element whose
corresponding data items are to be stored in the data buffer; an interface mechanism for
controlling the transfer of data items between the at least one channel and the data slots of
the data link in dependence upon said control data; and a memory interface for coupling
the controller to a memory, to enable data items to be transferred between the memory
and the at least one channel, wherein data items are represented as a fixed size when
transferred in the data slots, and each control register has a field settable to indicate the
actual size of each data item stored in the associated data buffer, thereby enabling the
memory interface to convert the data items between the actual size and the fixed size.

Claims 14 and 22 are allowable over the prior art of record since the cited references

taken individually or in combination fail to particularly teach or fairly suggest a method

of controlling interfacing to a data link, the data link enabling data items relating to a

number of data elements to be transferred in corresponding data slots of the data link, the

controller comprising: at least one channel, each channel comprising a data buffer for

storing data items, and a control register associated with the data buffer and arranged to

store control data, the control data settable to identify at least one data element whose

corresponding data items are to be stored in the data buffer; an interface mechanism for

controlling the transfer of data items between the at least one channel and the data slots of

the data link in dependence upon said control data; and a memory interface for coupling

the controller to a memory, to enable data items to be transferred between the memory

and the at least one channel, wherein the control data within the control register specifies

the number of data elements whose data items are stored in the associated data buffer,

and the memory interface is arranged to control the rate of transfer of data between the

data buffer and the memory dependent on the control data.

Response to Arguments

7.   The Examiner apologizes that after reviewing a case and a prior art the rejection appear

to be justified.

Conclusion

8.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

-   US Patent (6529975) to Miller et al discloses addressing and controlling expansion

    devices through an AC-link and a codec

-   US Patent (6434633) to Braun et al discloses facilitating AC-link communications

    between a controller and a slow peripheral of a codec

-   US Patent (5974480) to Qureshi et al discloses DMA controller which receives size

    data for each DMA channel

9.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Hong Cho whose telephone number is 571-272-3087.

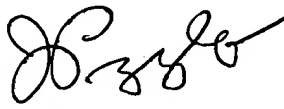The examiner can normally be reached on Mon-Fri during 7 am to 4 pm.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-3088.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

hc
Hong Cho
Patent Examiner
5/18/2005

JOHN PEZZLO
PRIMARY EXAMINER